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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/539,104	06/15/2005	Otto Steinbusch	US02 0610 US	9255
24738	7590	10/20/2006	EXAMINER	
PHILIPS ELECTRONICS NORTH AMERICA CORPORATION INTELLECTUAL PROPERTY & STANDARDS 1109 MCKAY DRIVE, M/S-41SJ SAN JOSE, CA 95131			MERANT, GUERRIER	
			ART UNIT	PAPER NUMBER
			2138	

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/539,104	STEINBUSCH, OTTO
	Examiner Guerrier Merant	Art Unit 2138

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 15 December 2003.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-15 is/are pending in the application.
 - 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-15 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 06/15/05 is/are: a) accepted or b) objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>20051215</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This is the initial office action based on the application filed on December 15, 2003. Claims 1-15 are currently pending and have been considered below.

Drawings

2. The drawings are objected to under 37 CFR 1.83(b) because they are incomplete. 37 CFR 1.83(b) reads as follows:

When the invention consists of an improvement on an old machine the drawing must when possible exhibit, in one or more views, the improved portion itself, disconnected from the old structure, and also in another view, so much only of the old structure as will suffice to show the connection of the invention therewith.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the

changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

- a. (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Casseti et al. (US 6,311,302 B1).

5. Claim 1: Casseti et al. (US 6,311,302 B1) discloses a method of coupling a plurality of test access port (TAP) controllers to a single external interface (col. 3, lines 6-19, see *fig. 1*), comprising: resetting a first bit in each of plurality of TAP controllers (col. 3, lines 20-37) a known state (*on/off*); producing a first signal based, at least in part, on the state of the first bit in each of the plurality of TAP controllers (*depending upon the command loaded into the internal TLM register, the TLM module enables or disables various TAPs in a system by controlling TMS-* col. 2, lines 21-50); selecting one of the plurality of TAP controllers based, at least in part, on the first signal (*this functionality is done by the Chip-level TML 40- see figs. 1 or 2*); coupling an external input terminal to an input terminal of the selected one of the plurality of TAP controllers;

and coupling an output terminal of the selected one of the plurality of TAP controllers to an external output terminal (*col. 4, lines 53-65*).

6. Claim 2: The method of claim 1, wherein the TAP controller comprises a finite state machine and a plurality of registers (*col. 5, lines 7-28*).

7. Claims 3 and 4: Casseti et al. discloses a method as in claim 2 above, further comprising toggling (*inverting*) the first bit in the selected one of the plurality of TAP controllers; and repeating steps (b) through (e) (*col. 5, lines 56-67 & col. 6, lines 1-10*).

8. Claims 5 and 6: Casseti et al. discloses a method as in claim 3 above, wherein the plurality of TAP controllers are disposed on a single integrated circuit and the first signal is produced within the single integrated circuit (see *figs. 1 & 2 for connection-* *col. 4, lines 53-68 & col. 5, lines 1-6*).

9. Claim 7: Casseti et al. discloses a method as in claim 6 above, further comprising receiving from a source external to the single integrated circuit, a clock signal (see *figs 1& 2 wherein externals signals TCK, TMS, TDI, TRST are being received by the integrated circuit 10*).

10. Claims 8-10, 12 and 13: Casseti et al. discloses an integrated circuit (*item 10, Figs. 1 & 2*), comprising: a plurality of functional blocks (*items 12 & 14, Figs. 1 & 2*),

each functional block having a test access port (TAP) controller coupled thereto (*items 16, 18, 30, 32- Figs. 1 & 2*); each TAP controller including a first register bit (*items 20 & 36- Figs. 1 & 2*), each first register bit adapted to produce a known output state in response to a reset signal (*depending upon the command loaded into the internal TLM register which is resetting after each instruction, the TLM module enables or disables various TAPs in a system by controlling TMS- col. 2, lines21-50*), each first register bit further adapted to toggle in response to a register write operation; and routing logic (*CTLM, item 40; fig. 1&2*) adapted to selectively provide, based at least in part on the state of the plurality of first register bits, a communication path between an external input signal source and an input terminal of a selected one of the TAP controllers (*col. 5, lines 56-67 & col. 6, lines 1-10, see Figs. 1&2*).

11. Claim 11: Casseti et al. discloses an integrated circuit as in claim 9 above, wherein a transition between the selectively provided communication paths is transparent to an external observer (*col. 4, lines 53-66- once an instruction is loaded, the TLM 40 selects which Tap to access without the help of user or observer*).

12. Claim 14: Casseti et al. discloses an integrated circuit as in claim 13 above, wherein the each of the plurality of TAP controllers has a second input terminal adapted to receive a clock signal (*TCK, fig. 1*), a third input terminal adapted to receive mode select signal (*TMS, fig.1*), and a fourth input terminal adapted to receive a reset signal (*TRST, fig.1*); wherein the plurality of second input terminals are coupled in common,

the plurality of third input terminals are coupled in common, and the plurality of fourth input terminals are coupled in common (*col. 5, lines 7-28*).

13. Claim 15: Casseti et al. discloses an integrated circuit of claim 14 above, further comprising a chain bit (*item 22 figs. 1& 2*) disposed in a first one of the plurality of TAP controllers.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- a) Whetsel (US 6,804,725) discloses a TAP linking module to control and access of plural TAPs on an IC through one set of JTAG signal pins.
- b) Adusumilli et al. (US 6,385,749) discloses a method and arrangement for controlling multiple test access port control modules.
- c) Joshi et al. (US 6,968,408) discloses Linking addressable shadow port and protocol for serial bus networks.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Exr. Merant Guerrier whose telephone number is (571) 270-1066. The examiner can normally be reached Monday through Thursday from 10:30 a.m. to 3:30 p.m.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. Draft or informal faxes, which will not be entered in the application, may be submitted directly to the examiner at (571) 270-2066.



Guerrier Merant
10/10/06



ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100